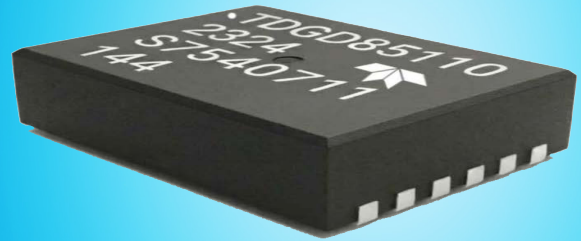


TDGD85110EP

Technical Specifications

Discrete GaN Transistor Driver

Isolated Single-Channel GaN Driver with Power-Thru



Description

The TDGD85110EP isolated gate driver is optimized for driving GaN transistors in multiple applications and topologies. An isolated output bias supply is integrated into the driver, eliminating the need for any external gate drive auxiliary bias supply or high-side bootstrap. (continued on page 2)

Applications

- Military temperature range dc-dc Converters
- Battery Management Systems
- Power Supplies
- Motor Control Systems
- High efficiency power conversion
- High density power conversion
- ac-dc Converters
- Bridgeless Totem Pole PFC
- ZVS Phase Shifted Full Bridge
- Half & Full Bridge topologies
- Synchronous Bucks or Boosts
- Uninterruptible Power Supplies
- Motor Drives
- Fast Battery Charging
- On Board Battery Chargers
- E-Switch

Typical Features

- Transformer Isolation barrier
- Power-Thru integrated isolated bias -
 - No need for high-side bootstrap
 - No need for external secondary-side bias
- 50 ns propagation delay
- Separate drive output pins: pull-up (2.8 Ω) and pull-down (1.0 Ω)
- Supply voltage 7 V < VDRV < 13.2 V
- Undervoltage lockout on primary VDRV and secondary VSEC
- Enable pin with fast response
- Continuous ON capability—no need to recycle IN or recharge bootstrap capacitor
- CMTI > 100 V/ns dv/dt immunity
- Creepage distance 8.4 mm
- Safety Regulatory Approvals -
 - 5 kV RMS VISO per UL 1577
 - 7 kV pk VIOTM maximum transient isolation voltage
 - 1 kV pk maximum working isolation voltage
- SEL pin selects between 6.7 V and 10 V UVLO
- -55 °C - 125 °C operation
- Matched propagation delay (≤ 10 ns) from part-to-part
- Package: 10 mm x 7.66 mm 12-pin, low profile SMT

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Description (continued)

This greatly simplifies the system design and reduces EMI through reduced total common-mode (CM) capacitance. It also allows the driving of a floating switch in any location in a switching power topology. The driver has fast propagation delay and high peak source/sink capability to efficiently drive GaN transistors in high-frequency designs. High CMTI combined with isolated outputs for both bias power and drive make it ideal in applications requiring isolation, level-shifting, or ground separation for noise immunity. The device is available in a compact low-profile surface-mount NH package. Several protection features are integrated, including undervoltage lockout on primary and secondary bias rails, internal pull-down on IN pin and OUTPD pin, fast response enable input, and OUT pulse synchronization with first IN rising edge after enable (avoids asynchronous runt pulses).

Typical Application

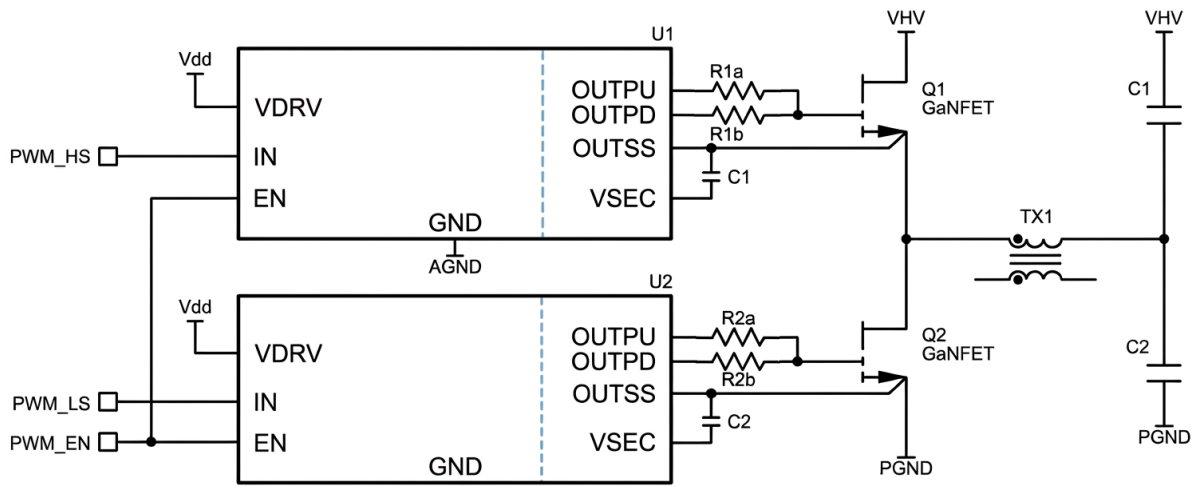


Figure 1: Typical TDGD85110EP half-bridge application-eliminates high-side bootstrap

Ordering Information

Ordering Code	Switch	# of Channels	Output	Package	Tape and Reel Details
TDGD85110EP	E-mode GaN	1	Unipolar	10 mm x 7.66 mm x 2.41 mm, 12-pin, low profile SMT	13-inch, 1,500 pieces

Absolute Maximum Ratings ⁽¹⁾

Characteristics	Symbol	Notes	Rating	Units
Drive Supply Voltage	DRV	VDRV, wrt to GND	- 0.5 to 15	V
Input Data	IN	IN, wrt to GND	- 0.5 to 15	V
Enable	EN	EN, wrt to GND	- 0.5 to 15	V
Select	SEL	SEL, wrt GND	- 0.5 to 15	V
Output Drive Pull-Up	OUTPU	OUTPU to OUTSS	- 0.5 to 15	V
Output Drive Pull-Down	OUTPD	OUTPD to OUTSS	- 0.5 to 15	V
Isolated Bias Supply	SEC	VSEC to OUTSS	- 0.5 to 15	V
Junction Temperature	T _J		-55 to 150	°C
Storage Temperature	STG		-55 to 150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

Parameter	Symbol	Value	Units
Human body model	V _{HBM}	±2	kV
Charged device model	V _{CDM}	±500	V

Thermal Characteristics (May require derating at maximum conditions; see application information)

Parameter	Symbol	Value	Units
	See Note (1)		
Thermal Resistance (junction-to-ambient)	R _{θJA}	102	°C/W

⁽¹⁾ Additional thermal information available on the Teledyne website.

Recommended Operating Conditions: Valid at $-55\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$, $7\text{ V} < V_{\text{DRV}} < 13.2\text{ V}$, $C_{\text{SEC}} = 22\text{ nF}$, $C_{\text{OUT}} = 1\text{ nF}$, unless otherwise stated.

Characteristics	Symbol	Conditions	Min	Typ	Max	Units
SUPPLY VOLTAGE PINS						
Drive Supply Voltage	V_{DRV}		7	-	13.2	V
INPUT PINS						
Input Data	V_{IN}		V_{GND}	-	V_{DRV}	V
Enable Active High	V_{EN}		V_{GND}	-	V_{DRV}	V
Select	V_{SEL}		V_{GND}	-	V_{DRV}	V
OUTPUT PINS						
Output Pull-Up	V_{OUTPU}		0	-	13.2	V
Output Pull-Down	V_{OUTPD}		0	-	13.2	V
Isolated Supply Referenced to OUTSS	V_{SEC}		0	-	13.2	V
VSEC Pin Capacitor C_{SEC}	C_{SEC}	External capacitance connected between VSEC and OUTSS pins; external $C_{\text{OUT}} = 1\text{ nF}$	5 ^[1]	27	100 ^[2]	nF
Junction Temperature	T_J		-55	-	125	$^{\circ}\text{C}$

^[1] Smaller C_{SEC} values than the recommended typical value can give higher voltage ripple on C_{SEC} .

^[2] Larger C_{SEC} values will mean longer startup times.

Isolation Characteristics

Characteristics	Symbol	Test Conditions	Value	Units
GENERAL				
External Clearance	CLR	Shortest terminal-to-terminal distance through air	8.4	mm
External Creepage	CPG	Shortest terminal-to-terminal distance across the package surface	8.4	mm
Distance Through Insulation	DTI	Internal insulation thickness	200	μm
Comparative Tracking Index	CTI	According to IEC 60112	400 to 599	V
Material Group	MG	According to IEC 60664-1	II	
Overvoltage Category		Per IEC 60664-1 at 600 V line voltage	I-IV	
Maximum Reinforced Working Voltage ^{[1] [2]}	V_{IORM}	Maximum approved working voltage for basic insulation according to UL 62368-1:2014 (Edition 2)	1000	$V_{\text{PK}}, V_{\text{DC}}$
			700	V_{RMS}
Maximum Impulse Voltage	V_{IMP}	Tested to UL 62368 Table D1 circuit 3	8000	V_{PK}
Maximum Transient Isolation Voltage	V_{IOTM}	60 sec rating, 100% production test, 1 sec at 6000 V_{RMS}	7000	V_{PK}
Maximum Surge Isolation Voltage	V_{IOSM}	Tested to UL 62368 Table D1 circuit 3 in oil at 1.6 × rating	8000	V_{PK}

Isolation Characteristics (continued)

Characteristics	Symbol	Test Conditions	Value	Units
Partial Discharge	q_{PD}	Method 81: At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, $t_{ini} = 1$ s; $V_m = 1.875 \times V_{IORM}$, $t_m = 1$ s	≤ 5	pC
Barrier Capacitance, Input to Output	C_{IO}	$V_{IO} = 0.5 \times \sin(2\pi ft)$, $f = 1$ MHz	<1	pF
Insulation Resistance, Input to Output	R_{IO}		$>10^{12}$	Ω
Climatic Classification			40/105/21	
UL1577				
Withstand Isolation Voltage	V_{ISO}	60 sec rating, 100% production test, 1 sec at 6000 VRMS	5000	V_{RMS}

^[1] Pending certification to UL 62368 Edition 2

^[2] Working Voltage evaluated for use at Pollution Degree 2 and Material Group II

MSL Rating (see Notes)

Device	MSL Rating	Maximum Floor Life at Standard Ambient (30 °C / 60% RH)	Maximum Peak Reflow Temperature	Pre-Reflow Bake Requirement
TDGD85110EP	MSL-3	168 hours	260°C	Per JEDEC J-STD-033C

Notes: Per JEDEC J-STD-033C, the TDGD85110EP devices are rated MSL3. This MSL3 rating means that once the sealed production packaging is opened, the devices must be reflowed within a "floor-life" of 168 hours (1 week) if they are stored in standard ambient conditions (30 °C and 60% relative humidity (RH)).

The peak reflow temperature should not exceed the maximum specified in MSL Rating table. If the devices are exposed to the standard ambient for more than 168 hours, they must be baked before reflow to remove any excess moisture in the package and prevent damage during reflow soldering. The required bake times and temperatures are detailed in IPC/JEDEC standard J-STD-033C. If the devices are exposed to higher temperature and/or RH compared to the standard ambient of 30 °C / 60% RH, the floor-life will be shortened due to the increased rate of moisture absorption. If the actual ambient conditions exceed the standard ambient, it is recommended that parts should always be baked per IEC/JEDEC J-STD-033C before reflow as a precaution to avoid potential device damage during reflow soldering.

Functional Block Diagram

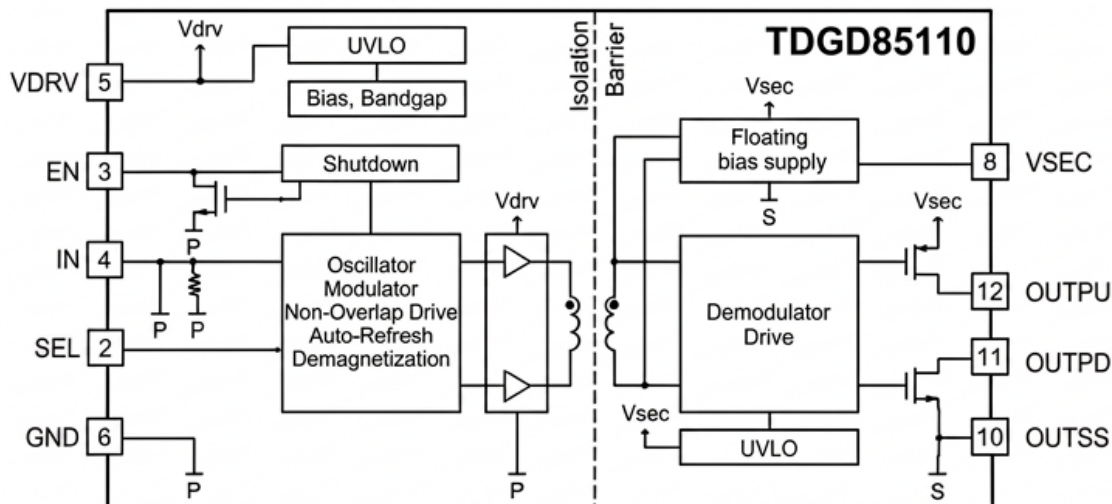


Figure 2: TDGD85110EP Block Diagram

Pinout Diagram and Terminal List Table



Figure 3: Package NH Pinout (Top View)

Terminal List Table

Number	Name	Function
1	GND	Internally connected to GND; recommend external connection to GND net (pin 6) to improve thermal impedance; can be left floating if necessary.
2	SEL	Tie to VDRV for a ~10 V UVLO or to GND for a ~6.7 V UVLO.
3	EN	Bidirectional enable pin. Tie to VDRV through a resistor to permit external circuitry to disable the driver chip; see Figure 4.
4	IN	PWM input; see Electrical Characteristics table.
5	VDRV	Ground referenced voltage supply. This voltage indirectly sets the output gate drive amplitude.
6	GND	Ground pin for input/primary side.
7	OUTSS	Internally connected to OUTSS; recommend external connection to OUTSS net (pins 9, 10) to improve thermal impedance; can be left floating if necessary; see Bipolar Output Drive section.
8	VSEC	External capacitor referenced to OUTSS.
9	OUTSS	Isolated output return pin.
10	OUTSS	Isolated output return pin.
11	OUTPD	Isolated output drive pull-down pin; see Electrical Characteristics table.
12	OUTPU	Isolated output drive pull-up pin; see Electrical Characteristics table.

Electrical Characteristics: Valid at $-55\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$, $7\text{ V} < V_{\text{DRV}} < 13.2\text{ V}$, $C_{\text{SEC}} = 22\text{ nF}$, $C_{\text{OUT}} = 1\text{ nF}$, unless otherwise stated.

Characteristics	Symbol	Test Conditions		Min	Typ	Max	Units
SUPPLY CURRENTS							
VDRV Disable Current	I DRV_DIS	V _{IN} = 0, EN = 0	SEL at GND	–	0.375	0.56	mA
			SEL at V _{DRV}	–	0.416	0.65	
VDRV Quiescent Current	I DRV_Q	V _{IN} = 0, EN = 1	SEL at GND	–	1.7	2.5	mA
			SEL at V _{DRV}	–	1.7	2.8	
VDRV Switching Current	I DRV_SW	F _S = 10 kHz, V _{DRV} = 10.5 V, EN = 1	SEL at GND	–	2.35	3.3	mA
			SEL at V _{DRV}	–	2.4	3.6	
VDRV Switching Current	I DRV_SW	F _S = 100 kHz, V _{DRV} =10.5 V, EN = 1	SEL at GND	–	6.8	11.7	mA
			SEL at V _{DRV}	–	6.85	12.2	
VDRV Switching Current	I DRV_SW	F _S = 400 kHz, V _{DRV} =10.5 V, EN = 1	SEL at GND	–	23.6	40.0	mA
			SEL at V _{DRV}	–	23.7	45.0	
INPUT PINS							
Input Data - Logic Low	V _{IN(L)}			–	–	0.8	V
Input Data - Logic High	V _{IN(H)}			2.0	–	–	V
Input Data Hysteresis	V _{IN(HYS)}			–	400	–	mV
Enable Active High - Logic Low	V _{EN(L)}			–	–	0.8	V
Enable Active High - Logic High	V _{EN(H)}			2.0	–	–	V
Enable Active High - Hysteresis	V _{EN(HYS)}			–	400	–	mV
Internal On-Chip Pull-Down Resistance On IN Pin	R _{IN}	TA = 25 °C		200	300	650	kΩ
OUTPUT PINS							
OUTPU Pull-Up Resistance	R _{PU}			1.5	2.8	3.6	Ω
OUTPD Pull-Down Resistance	R _{PD}			0.7	1.0	2	Ω
High Level Source Current ^[1]	I _{SOURCE}	V _{SEC} = 10 V, R _{ext_pu} = 0 Ω, C _{OUT} = 10 nF		–	2	–	A
Low Level Sink Current ^[1]	I _{SINK}	V _{SEC} = 10 V, R _{ext_pd} = 0 Ω, C _{OUT} = 10 nF		–	4	–	A
VGATE High	V _{GATE_H}	V _{DRV} = 7 V, SEL at GND		4.5	5.1	6.5	V
		V _{DRV} = 9 V, SEL at GND		5.5	6.5	7.2	
		V _{DRV} = 10.5 V		6.6	7.6	9	
		V _{DRV} = 13.2 V		8	9.6	11.4	

Electrical Characteristics (continued)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Units
OUTPUT PINS (continued)						
VGATE Low	V _{GATE_L}	V _{DRV} = 7 V, SEL = 0 V	-3	0.560	1.6	mV
		V _{DRV} = 9 V, SEL = 0 V	-3	0.545	1.4	
		V _{DRV} = 10.5 V	-3	0.532	1.3	
		V _{DRV} = 13.2 V	-3	0.515	1.2	
PRIMARY UNDERVOLTAGE LOCKOUT						
VDRV UV Threshold, Rising ^[2]	V _{DRV_UVH}	SEL at GND	6.5	6.7	6.9	V
		SEL at V _{DRV}	9.9	10.0	10.3	
VDRV UV Threshold, Falling	V _{DRV_UVL}	SEL at GND	6.1	6.3	6.4	V
		SEL at V _{DRV}	9.2	9.4	9.6	
VDRV UV Hysteresis	V _{DRV_UVHYS}	SEL at GND	0.45	0.48	0.49	V
		SEL at V _{DRV}	0.675	0.70	0.72	
SECONDARY UNDERVOLTAGE LOCKOUT						
VSEC UV Threshold, Rising	V _{SEC_UVH}		3.8	4.4	4.9	V
VSEC UV Threshold, Falling	V _{SEC_UVL}	TA = 25 °C	3.6	4.1	4.5	V
VSEC UV Hysteresis	V _{SEC_UVHYS}	TA = 25 °C	0.2	0.3	0.6	V

^[1] Not tested in production; guaranteed by design and bench characterization.

^[2] When VDRV is below the UVLO threshold, the driver output is actively held low.

Electrical Characteristics (continued)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Units
PROPAGATION TIMES						
Propagation Delay, High To Low, 7 V	t_{PHL_7V}	$R_{ext_pu} = 2\ \Omega$, $V_{DRV} = 7\ V$, $V_{SEL} = 0\ V$	–	70	85	ns
Propagation Delay, Low To High, 7 V	t_{PLH_7V}	$R_{ext_pd} = 2\ \Omega$, $V_{DRV} = 7\ V$, $V_{SEL} = 0\ V$	–	70	85	ns
Propagation Delay Match, 7 V	t_{PM_7V}	Part-to-part propagation delay difference, $V_{DRV} = 7\ V$, $V_{SEL} = 0\ V$	-10	–	10	ns
Propagation Delay, High To Low, 9 V	t_{PHL_9V}	$R_{ext_pu} = 2\ \Omega$, $V_{DRV} = 9\ V$, $V_{SEL} = 0\ V$	45	65	80	ns
Propagation Delay, Low To High, 9 V	t_{PLH_9V}	$R_{ext_pd} = 2\ \Omega$, $V_{DRV} = 9\ V$, $V_{SEL} = 0\ V$	50	65	80	ns
Propagation Delay Match, 9 V	t_{PM_9V}	Part-to-part propagation delay difference, $V_{DRV} = 9\ V$, $V_{SEL} = 0\ V$	-10	–	10	ns
Propagation Delay, High To Low, 10.5 V	$t_{PHL10V5}$	$R_{ext_pu} = 2\ \Omega$, $V_{DRV} = 10.5\ V$	47	50	75	ns
Propagation Delay, Low To High, 10.5 V	t_{PLH_10V5}	$R_{ext_pd} = 2\ \Omega$, $V_{DRV} = 10.5\ V$	45	50	75	ns
Propagation Delay Match, 10.5 V	t_{PM_10V5}	Part-to-part propagation delay difference, $V_{DRV} = 10.5\ V$	-10	–	10	ns
Propagation Delay, High To Low, 13.2 V	t_{PHL_13V2}	$R_{ext_pu} = 2\ \Omega$, $V_{DRV} = 13.2\ V$	44	50	72	ns
Propagation Delay, Low To High, 13.2 V	t_{PLH_13V2}	$R_{ext_pd} = 2\ \Omega$, $V_{DRV} = 13.2\ V$	45	50	72	ns
RISE AND FALL TIMES						
Rise Time, 7 V	t_r	$R_{ext_pu} = 2\ \Omega$, 20-80%, $V_{DRV} = 7\ V$, $V_{SEL} = 0\ V$	–	11	20	ns
Fall Time, 7 V	t_f	$R_{ext_pd} = 2\ \Omega$, 20-80%, $V_{DRV} = 7\ V$, $V_{SEL} = 0\ V$	–	11	20	ns
Rise Time, 9 V	t_r	$R_{ext_pu} = 2\ \Omega$, 20-80%, $V_{DRV} = 9\ V$, $V_{SEL} = 0\ V$	–	9	18	ns
Fall Time, 9 V	t_f	$R_{ext_pd} = 2\ \Omega$, 20-80%, $V_{DRV} = 9\ V$, $V_{SEL} = 0\ V$	–	9	12	ns
Rise Time, 10.5 V	t_r	$R_{ext_pu} = 2\ \Omega$, 20-80%, $V_{DRV} = 10.5\ V$, $V_{SEL} = V_{DRV}$	–	7	17	ns
Fall Time, 10.5 V	t_f	$R_{ext_pd} = 2\ \Omega$, 20-80%, $V_{DRV} = 10.5\ V$, $V_{SEL} = V_{DRV}$	–	7	11	ns
Rise Time, 13.2 V	t_r	$R_{ext_pu} = 2\ \Omega$, 20-80%, $V_{DRV} = 13.2\ V$, $V_{SEL} = V_{DRV}$	–	7	17	ns
Fall Time, 13.2 V	t_f	$R_{ext_pd} = 2\ \Omega$, 20-80%, $V_{DRV} = 13.2\ V$, $V_{SEL} = V_{DRV}$	–	7	12	ns
Shortest ON Time Allowable ^[1]	$t_{pw(on)}$	The ON time should never be less than specified minimum	–	–	–	ns
Shortest OFF Time Allowable ^[1]	$t_{pw(off)}$	The OFF time should never be less than specified minimum	–	–	–	ns

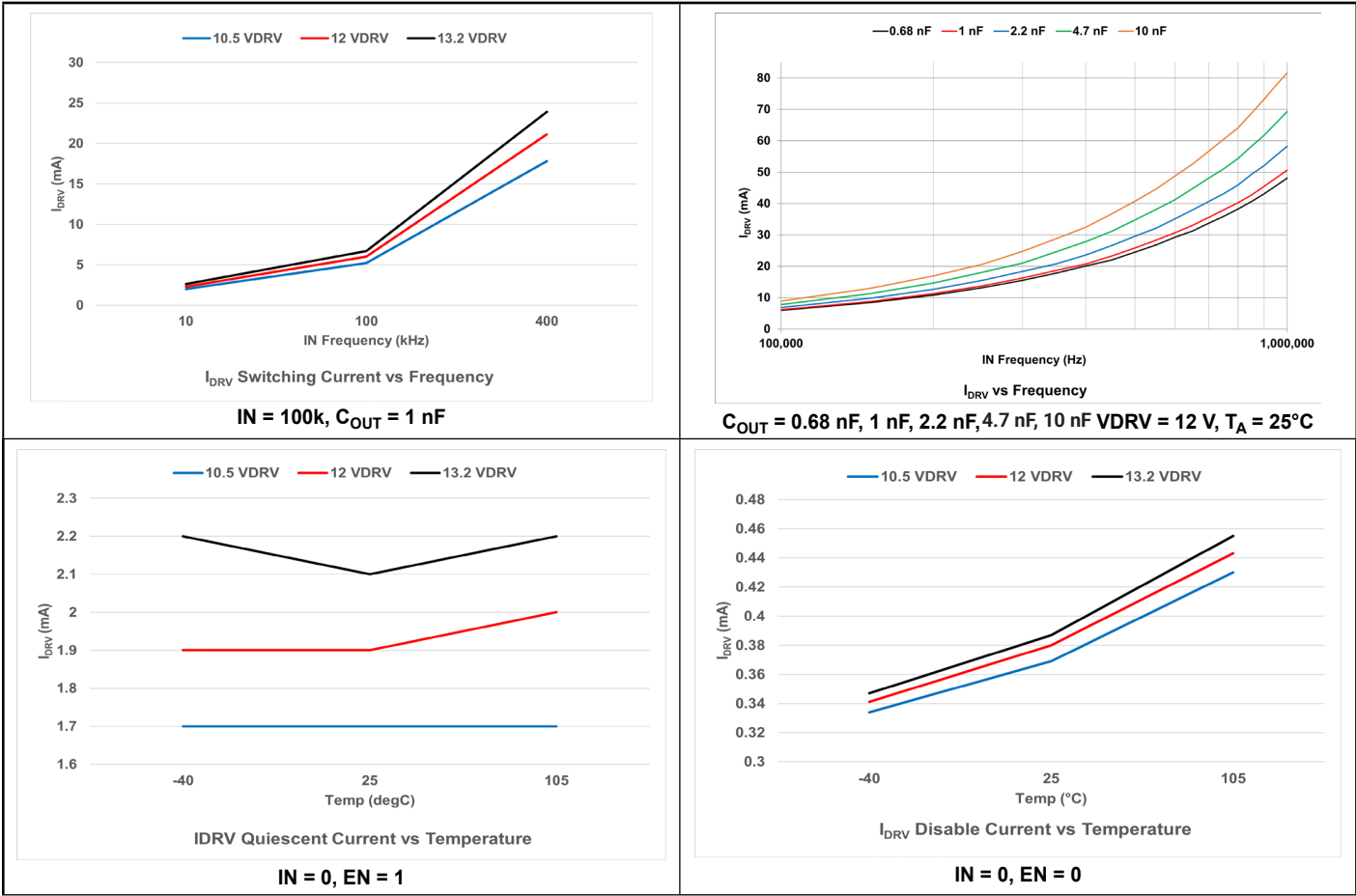
^[1] Not tested in production; guaranteed by design and bench characterization.

Electrical Characteristics (continued)

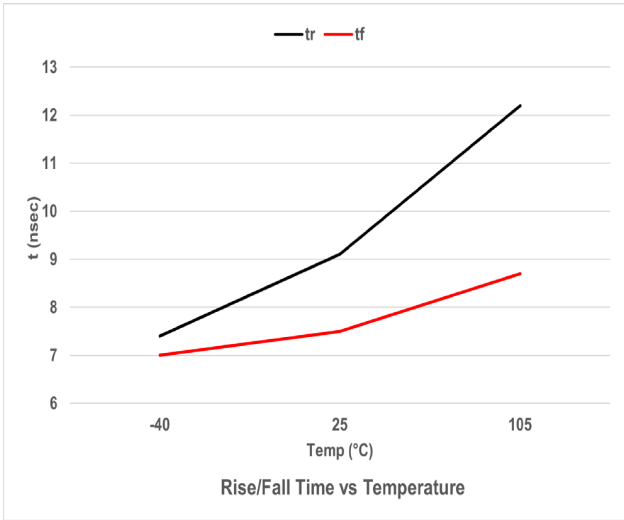
Characteristics	Symbol	Test Conditions	Min	Typ	Max	Units
STARTUP TIME						
Wait Time Before First IN Edge is Delivered After V _{DRV} is Within Specification	t _{START}		–	143	250	μs

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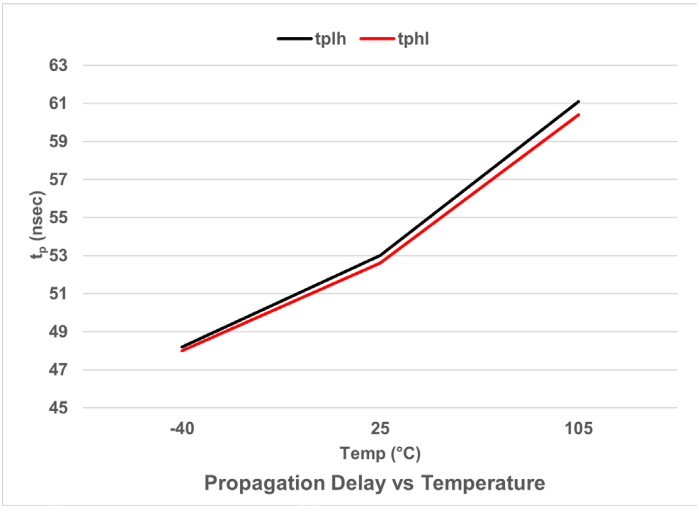
Typical IC Characteristics Curves ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)



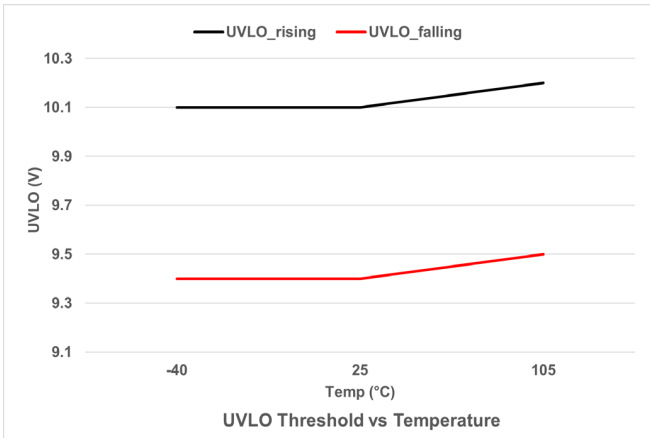
Typical IC Characteristics Curves (T_j = 25 °C Unless Otherwise Noted)



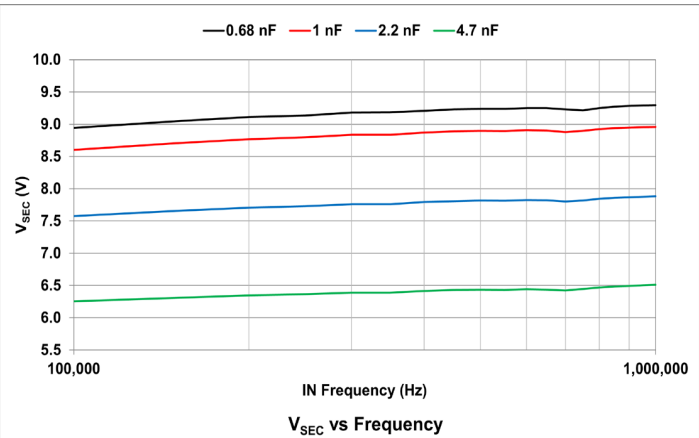
C_{OUT} = 1 nF, IN = PWM 100 kHz



C_{OUT} = 1 nF, IN = PWM 100 kHz



C_{OUT} = 1 nF, IN = 0



C_{OUT} = 1 nF, C_{SEC} = 20 × C_{OUT}, VDRV = 12 V

Functional Description

The TDGD85110EP is an isolated gate driver. Patented technology allows the transfer of both PWM signal and gate power across a single transformer-based isolation barrier. This eliminates the need to provide an isolated bias supply to power the isolated side of the driver, greatly simplifying the system design. Only an external decoupling capacitor is required on the isolated side.

The TDGD85110EP driver has been optimized for driving the gate of typical Schottky-gate Enhancement-mode (E-mode) GaN transistors, such as those available from GaN Systems, Innoscience, ST, Nexperia, GaN Power International, Taiwan Semiconductor, Rohm, and others. In addition, some Transphorm cascode-GaN devices can also be driven, where low-voltage logic-level MOS devices are used inside the cascode. An online FET selection tool can be downloaded from the Teledyne website to assist system designers to check compatibility of various FET devices with the driver. The maximum drive capability is 30 nC at 6 V VGS.

The isolated VSEC bias rail on the secondary is derived open-loop from the primary 12 V supply V_{DRV} . The VSEC rail level regulates quite well versus PWM switching frequency FSW at the IN pin for a given fixed V_{DRV} level and for a fixed load C_{OUT} at the OUTx drive pins (the load presented by the gate of the GaN HEMT being driven). This is because the charge delivered per PWM cycle naturally increases in tandem with the charge consumed by the transistor gate, so there is a good charge balance across a wide frequency range.

However, the VSEC rail does vary with effective loading of the gate of the transistor being driven; as the VSEC level falls, more charge is available to be delivered to the secondary side while the charge consumed by the transistor gate decreases with falling VSEC level. Therefore, the VSEC rail will droop as far as needed until the charge delivered matches the charge consumed. For this reason, it's also very important to minimize the amount of charge diverted into any external loads. For example, a very low bias power external circuit can be powered using VSEC, but the consumption should be minimal, to minimize the charge diverted away from the gate of the transistor. Similarly, if a gate-source pull-down resistor is desired on the load transistor (to prevent false turn-on in the case of a manufacturing fault, such as an open-circuit gate turn-on resistor), the resistor value should be as large as possible.

The recommended value is 100 kΩ, to minimize dc loading on VSEC. Since dc load current converts to equivalent charge as $Q = I \times t$, dc loading effects will become significantly more pronounced at lower PWM frequency, as the time duration 't' gets longer.

Since there is just a single magnetic isolation barrier to transfer both PWM signal and gate power, this also greatly reduces the total parasitic capacitance between the primary-side and isolated-side to typically < 1 pF total for both signal and power channels. This is much less than the typical total parasitic capacitance value for a solution using a conventional isolated gate driver with a separate isolated dc-dc bias supply in which the capacitance contribution from the dc-dc isolation transformer could be as high as 10 pF or more. This reduction in isolation capacitance greatly reduces the level of noise injected back into the low-voltage control circuit by the high-voltage and high dv/dt switching nodes in the power stage half-bridge legs, reduces system level Common-Mode (CM) EMI, and saves on power loss that occurs through repetitive charging and discharging of this parasitic capacitance between the high bus voltage level and ground.

Applications Information

UVLO Selection SEL Pin

The SEL pin sets the UVLO to about 10 V when tied to V_{DRV} or 6.7 V when at GND. It must be tied to GND for low-voltage operation.

Bidirectional Enable/Disable EN Pin

EN is a bidirectional open-drain pin which requires an external resistor pull-up to the V_{DRV} pin. The EN pin allows for management of startup and fault conditions between the PWM controller and multiple drivers through use of a shared enable EN line.

Either the PWM controller or the driver can pull the EN pin low via the EN bus, as shown in Figure 3. When the EN pin is pulled low (either externally or internally), the driver is forced into a mode in which the IN pin signal is ignored and the OUT pins are disabled and actively pulled low. When the EN pin goes high, normal driver operation is enabled.

In the event of an internal driver fault condition, such as UVLO or normal startup delay, the EN pin is actively pulled low internally by the driver. This driver pull-down can be detected by the PWM controller and used as a flag for an external fault, or to flag that the driver is ready, and PWM can commence.

The shared EN line is typically wired-AND with the controller EN pin, as shown in Figure 3. Multiple drivers can be connected in parallel with the controller on the shared EN line, such that all connected drivers will hold the EN line low until all drivers and the PWM controller have released their own EN pin, ensuring smooth safe startup of the system.

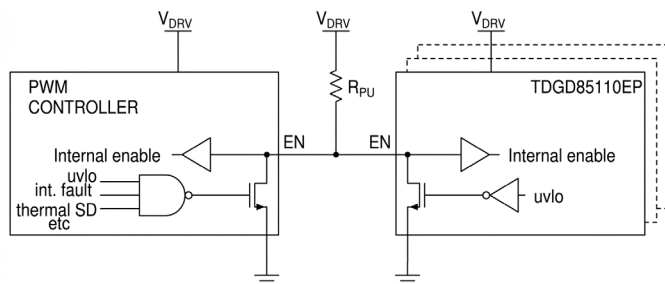


Figure 3: Example 'Wired-AND' connection between driver and controller

Note that the EN pin has no internal pull-up or pull-down—the open-drain configuration relies on an external pull-up resistor for normal operation. Similarly, the EN pin must be actively pulled low externally to disable the driver.

The EN pin should never be left floating or connected directly to V_{DRV} or any other system bias voltage; a pull-up resistor must be used. The EN pin should be connected to V_{DRV} through a pull-up resistor in a recommended range of 10 to 100 k Ω . The EN pin dv/dt when being pulled low or high should be at least 0.1 V/ μ s. When the EN pin is pulled low, the driver output is disabled and the OUTPD pin is pulled low, regardless of the IN pin level (high or low). The driver goes to a low-power standby mode and the isolated VSEC bias rail is allowed to discharge. The rate of decay of V_{SEC} depends on the value of the C_{SEC} capacitor. When the EN pin is subsequently pulled high, the driver will re-enable and the isolated VSEC bias rail will start to recharge. Even if the IN pin is connected to a PWM signal, the OUT pins will not respond until the V_{SEC} exceeds the secondary UVLO threshold. The rate of rise of V_{SEC} depends on the PWM frequency at the IN pin. Worst-case slowest rise time is when IN = 0, using the slowest internal energy-transfer mode. In this mode, the rise time will be approximately 250 μ s for C_{SEC} of 47 nF to charge from zero to the rising UVLO threshold.

Startup and Shutdown Procedure

Any PWM signal applied to IN must remain low until $V_{DRV} >$ UVLO threshold to avoid parasitic charging of the V_{DRV} rail through the IN pin internal ESD structures. After V_{DRV} exceeds the UVLO rising threshold, a startup time delay t_{START} is required to allow all internal circuits to initialize and stabilize. During t_{START} , any IN signal inputs are ignored. EN internal pull-down will remain active during t_{START} and will disable (i.e., go open-drain) only when V_{DRV} has reached its UVLO voltage level, all on-chip voltages are stabilized, and the internal t_{START} timer has elapsed. Thus, the EN pin can be used via a shared EN line to flag when t_{START} has elapsed, and the driver is ready to respond to PWM signals at the IN pin. Typical startup waveforms are shown in Figure 4

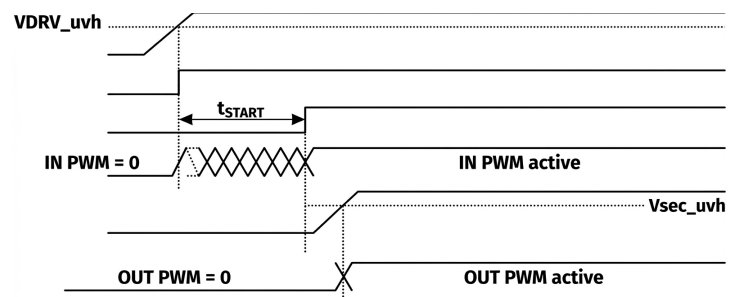


Figure 4: TDGD85110EP Startup Mechanism

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Once V_{DRV} drops below the UVLO falling threshold, the enable signal is pulled down and the driver output shuts down. The rate of decay of V_{SEC} is determined by the C_{SEC} capacitance as shown in Figure 5.

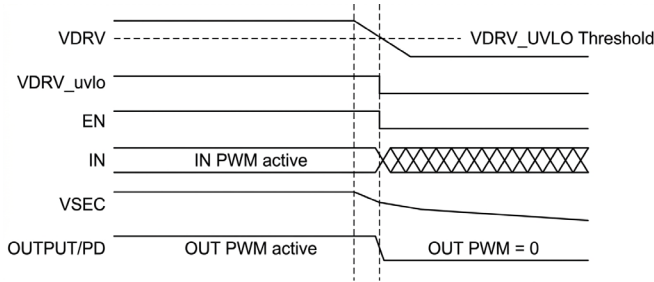


Figure 5: Shutdown Mechanism

Refresh Pulse Mechanism

In cases in which the IN PWM signal frequency is low or when IN is set to a continuous 1 or 0, in order to prevent V_{SEC} voltage decay the TDGD85110EP implements an internal clock of 12 μs ($T_{REFRESH}$). When $T_{REFRESH}$ elapses, the driver recharges the VSEC rail to maintain its output voltage. This condition persists until IN changes state as shown in Figure 6.

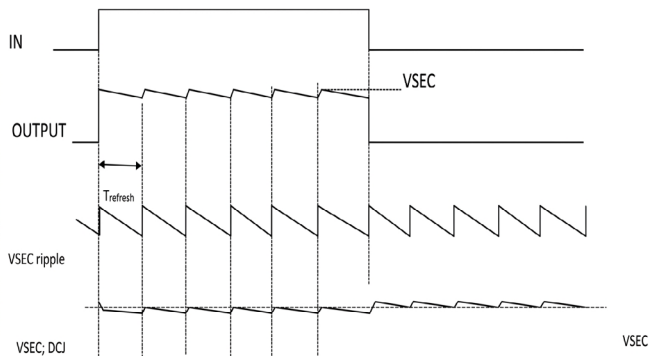


Figure 6: TDGD85110EP Refresh Mechanism

Operating Frequency and Thermal Derating

The maximum recommended PWM frequency is 1 MHz. However, the device internal dissipation, application PCB layout and ambient temperature must also be taken into account to ensure that the internal recommended $T_J(\text{MAX})$ of 125°C is not exceeded. Based on the application PWM frequency and the load transistor total gate charge $Q_{G(TOT)}$, the maximum allowed ambient temperature can be estimated using the curves in Figure 7 and a few simple calculations.

These curves are based on the device thermal performance using JEDEC-standard PCB footprint and PCB design (layer count and size of copper planes for heatsinking). The actual thermal performance in the end system design should always be verified, since every system is different in terms of exact PCB design and ambient airflow from natural or forced convection.

Because of the required creepage distance under the IC package to meet system safety requirements, putting a large copper plane under the IC for heatsinking purposes is not allowed. Instead, it's recommended that the primary-side GND pins and secondary-side OUTSS pins be connected to appropriate ground planes on each side, and to maximize the size of these planes to maximize thermal performance. Multiple thermal vias to larger inner-layer ground planes can also help improve thermal performance.

The effective gate capacitance C_{OUT} that loads the OUTx drive pins can be estimated from the GaN HEMT datasheet. The transistor total charge $Q_{G(TOT)}$ is usually specified in nC, for a given V_{GS} voltage swing.

$$C_{OUT} = \frac{Q_{G(TOT)}}{V_{GS}}$$

Knowing the value of C_{OUT} , the expected level of the secondary supply rail VSEC can be estimated from figure 8. From C_{OUT} , V_{SEC} , and the required PWM frequency F_{SW} , the total gate power can be calculated as follows:

$$P_{GATE} = F_{SW} \times C_{OUT} \times V_{SEC}^2$$

In practice, the system design will likely use external gate resistors to control the transistor turn-on and turn-off speed. The gate-drive power consumption P_{GATE} will be dissipated by the internal driver FET resistances and the external resistors apportioned by the ratio of the resistances. The larger the value of the external resistors, the higher the power dissipation in those resistors, and the lower the dissipation in the internal driver resistances. To simplify the thermal estimates and to add in design margin, it is assumed that all the P_{GATE} power is dissipated inside the driver package.

The internal driver stage MOSFETs will consume drive power, and they will have switching losses, so there is an efficiency factor that needs to be accounted for when

Applications Information

estimating the internal power consumed when delivering the P_{GATE} power.

Finally, the internal isolated bias power stage consumes power. As well as the IC quiescent power consumption, there are also drive, conduction, and switching losses in the internal power FETs that drive and rectify the energy transfer through the internal isolation transformer, as well as the conduction and core losses of the transformer. These losses scale approximately linearly with PWM frequency.

Combining all of these loss mechanisms, the total package power dissipation (in mW) can be estimated using the following empirical formula, where F_{SW} is in kHz and P_{GATE} is in mW. This assumes a fixed V_{DRV} level of 12 V.

$$P_{DISS} = 0.58 \times F_{SW} + \frac{P_{GATE}}{0.7}$$

Using the standard JEDEC thermal impedances in the thermal characteristics table, the maximum allowed ambient temperature T_A can be estimated from:

$$T_{A(MAX)} = T_{J(MAX)} - P_{DISS} \times R_{TH(JA)}$$

Alternatively, Figure 7 below can be used to graphically estimate the allowable $T_{A(MAX)}$ as a function of F_{SW} and C_{OUT} . The online transistor selection tool can also be used to estimate expected driver temperature rise over ambient, and maximum allowed T_A .

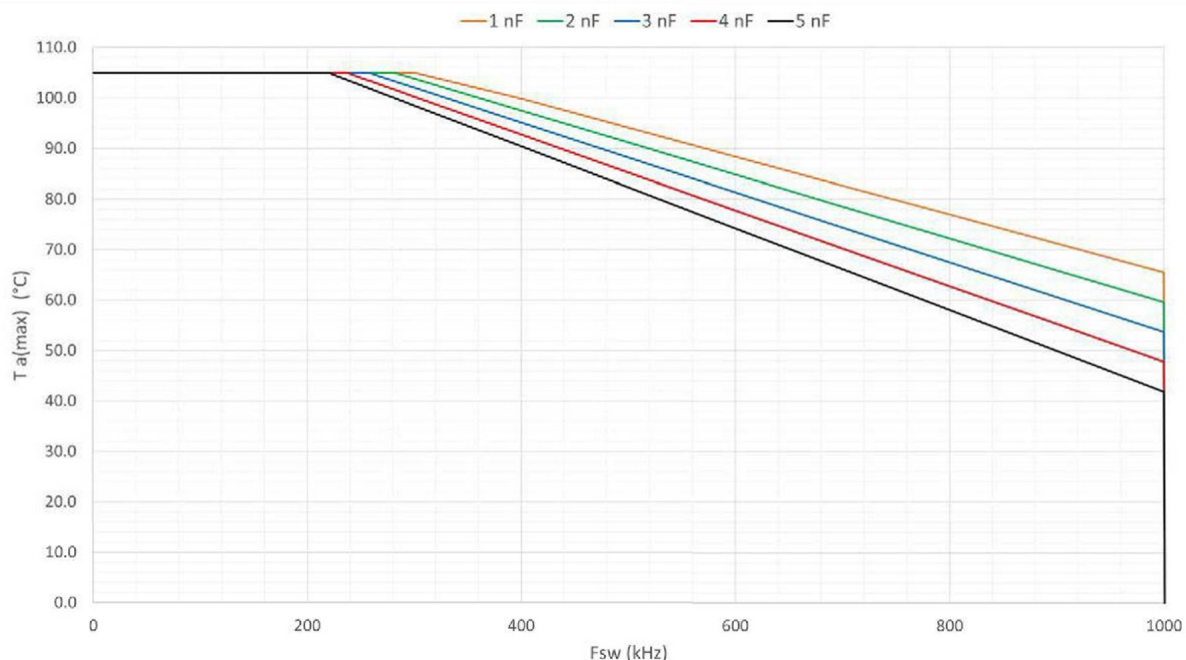


Figure 7: TDGD85110EP thermal derating curve as a function of load capacitance C_{OUT} and PWM frequency F_{SW}

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WORKED EXAMPLE

What follows is an example calculation based on Teledyne TDGDEK85110KNH-01-T-MH evaluation board. Assume the target switching frequency is 400 kHz, V_{DRV} is 12 V, and the required maximum ambient temperature is 85 °C.

The transistor used on the board is a GS-66516-B from GaN Systems. From the GaN datasheet, the $Q_{G(TOT)}$ is specified at 14.2 nC at 6 V V_{GS} swing. Therefore, the equivalent C_{OUT} is

$$C_{OUT} = \frac{14.2 \text{ nF}}{6} = 2.37 \text{ nF}$$

From Figure 8, for this value of C_{OUT} the V_{SEC} level can be estimated as approximately 7.5 V. Note that this evaluation board uses an external Zener circuit to limit the positive V_{GS} swing to approximately 6.2 V, with the balance of the V_{SEC} voltage appearing as a negative V_{GS} in the off-state. Nevertheless, the full V_{GS} swing must be used to estimate the gate power dissipation.

$$P_{GATE} = 400 \text{ kHz} \times 2.37 \text{ nF} \times 7.5^2 \text{ V} = 53 \text{ mW}$$

From this, the total package power dissipation can be estimated:

$$P_{DISS} = 0.58 \times 400 + \frac{53 \text{ mW}}{0.7} = 308 \text{ mW}$$

Now the maximum allowed ambient temperature can be verified to ensure that it meets the system requirement:

$$T_{A(MAX)} = 125 \text{ }^{\circ}\text{C} - \left(0.308 \text{ W} \times 102 \frac{^{\circ}\text{C}}{\text{W}} \right) = 93.6 \text{ }^{\circ}\text{C}$$

This equation shows that the design can meet the required maximum ambient temperature. However, as noted above, this uses $R_{\theta(JA)}$ estimates based on standardized JEDEC footprints and PCB layouts; the actual thermal performance must be verified in each individual application.

The maximum allowed ambient temperature can also be readily estimated from the curves in Figure 7. Using F_{SW} of 400 kHz and C_{OUT} of approximately 2.4 nF, the estimated $T_{A(MAX)}$ is approximately 96 °C, which is close to the calculated result using the empirical loss estimation.

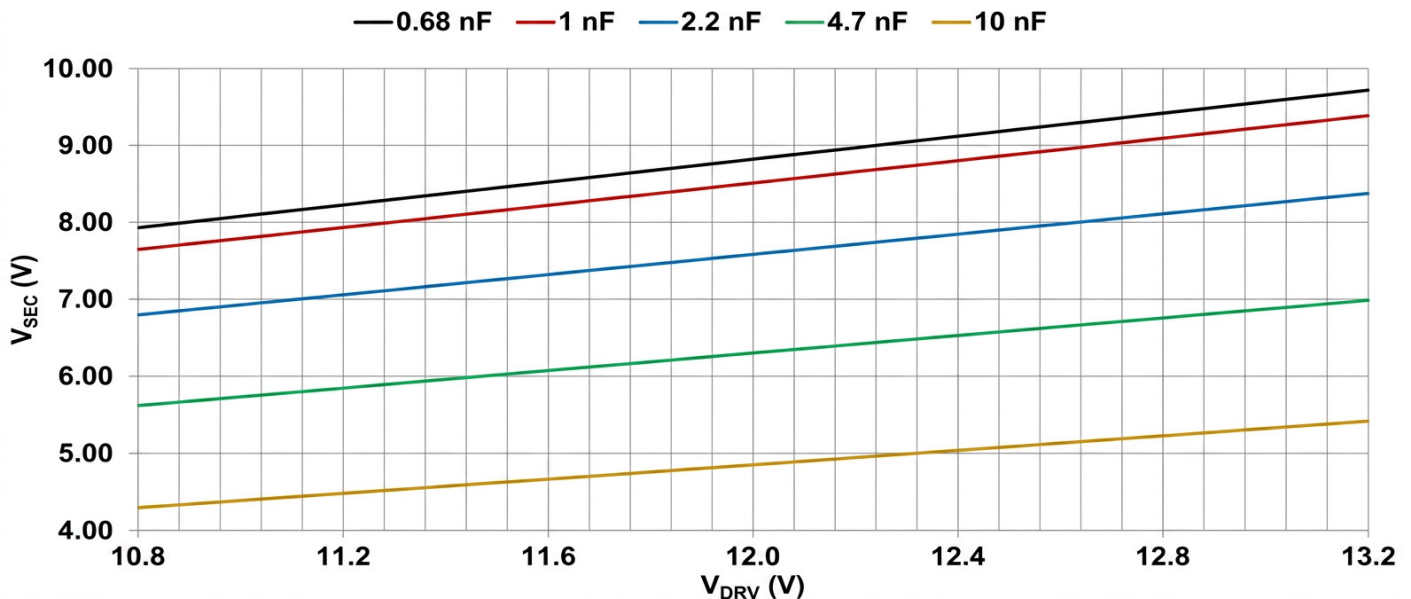


Figure 8: Typical V_{SEC} versus V_{DRV} for five C_{OUT} capacitors; Conditions: F_{IN} =100 kHz, D = 50%, C_{SEC} = 20 x C_{OUT}

Applications Information

V_{SEC} , V_{DRV} , and C_{SEC} Design Guidelines

The output gate drive rail V_{SEC} is always less than V_{DRV} due to internal impedances and voltage drops. The V_{SEC} level depends on factors such as V_{DRV} level, C_{OUT} , and C_{SEC} . Figure 8 shows the typical output V_{SEC} level as a function of V_{DRV} and C_{OUT} for an assumed value of C_{SEC} as a multiple of C_{OUT} for a 50% duty cycle PWM at the IN pin.

C_{OUT} is the equivalent load capacitance presented by the total gate charge of the transistor being driven at the OUTx pins, as given in the previous equation calculating C_{OUT} .

In some cases in which the load transistor gate charge is quite low, the V_{SEC} level may be higher than required. In order to reduce the V_{SEC} level to suit the transistor V_{GS} requirements, the following steps can be taken:

- Make use of the recommended external Zener clamping circuit to limit the positive V_{GS} swing (with the balance appearing as a negative off-state V_{GS}). See section “Bipolar Output Drive” for more details.
- Reduce V_{DRV} level somewhat, to reduce V_{SEC} . This might require tying SEL low to take advantage of the lower UVLO.
- Add extra load capacitance across the transistor gate-source terminals to increase the effective load gate charge and reduce V_{SEC} .
- Add some limited dc loading on the VSEC rail. This can be achieved by a pull-down resistor across the transistor gate-source terminals, or a load resistor from VSEC pin to OUTSS pin. The resistor value should be kept quite large in order to not overload V_{SEC} excessively. Start with a large value $>100\text{ k}\Omega$, and gradually decrease until the desired V_{SEC} level is achieved.

The recommended value for C_{SEC} is approximately 10 to 20 times C_{OUT} (the equivalent gate capacitance), to give approximately 5% to 10% switching ripple on the VSEC rail. Other values can be used; however, lower values will result in higher ripple. Larger C_{SEC} will require a longer startup time. The maximum recommended value of $C_{SEC} = 100\text{ nF}$ should not be exceeded.

Since power is transferred to the secondary at a rate proportional to the PWM frequency, and the gate power consumed by the load transistor is also proportional to frequency, the VSEC rail is relatively well regulated as PWM frequency is varied, for a given fixed V_{DRV} and fixed C_{OUT} . This is illustrated in Figure 9.

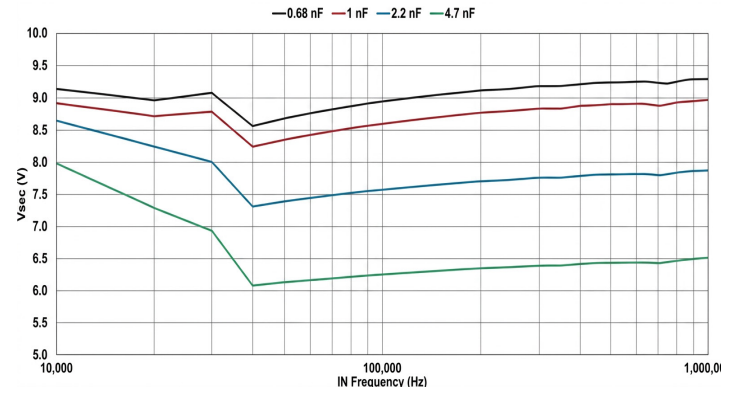


Figure 9: V_{SEC} vs. Frequency

Bipolar Output Drive

Bipolar output drive is used to provide a negative gate voltage, as shown in Figure 10. This can be beneficial in protecting against false turn on due to parasitic circuits components. It can be added simply to the TDGD85110EP by including three extra small external components.

The 6.2 V Zener clamps the amplitude of the positive V_{GS} swing during the on-time, with the balance of the V_{SEC} voltage appearing as a negative V_{GS} during the off-time. The 3.6 k Ω resistor in series with the Zener should be kept relatively large so that it does not load the VSEC rail excessively.

For full details, please see the Teledyne HiRel application note AppN85110-8_072026, “FET Gate Drive and Bipolar Output Applicable TDGD85110EP Gate Drivers.”

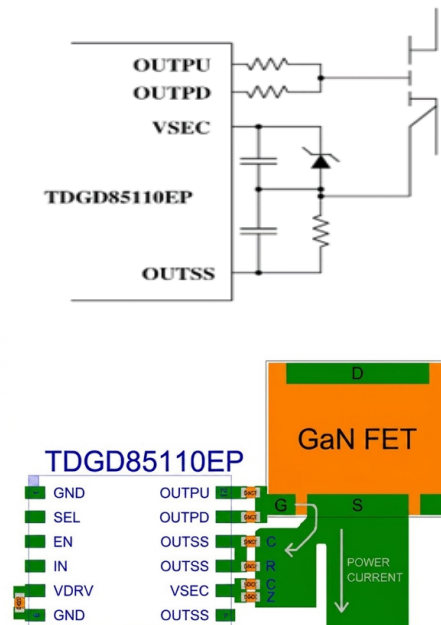


Figure 10: TDGD85110EP bipolar drive and recommended PCB layout

Typical Applications

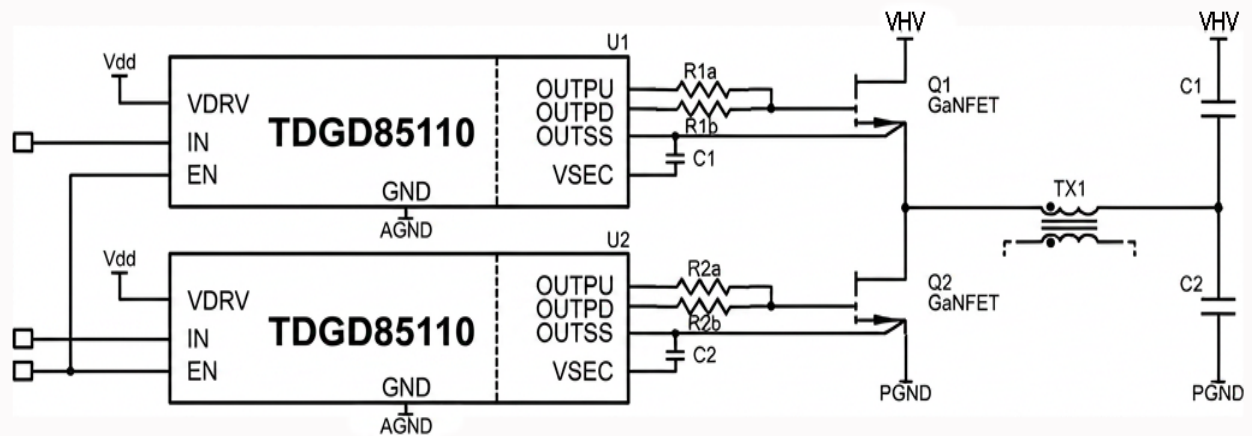


Figure 11: Half-bridge with TDGD85110EP as high and low side drivers

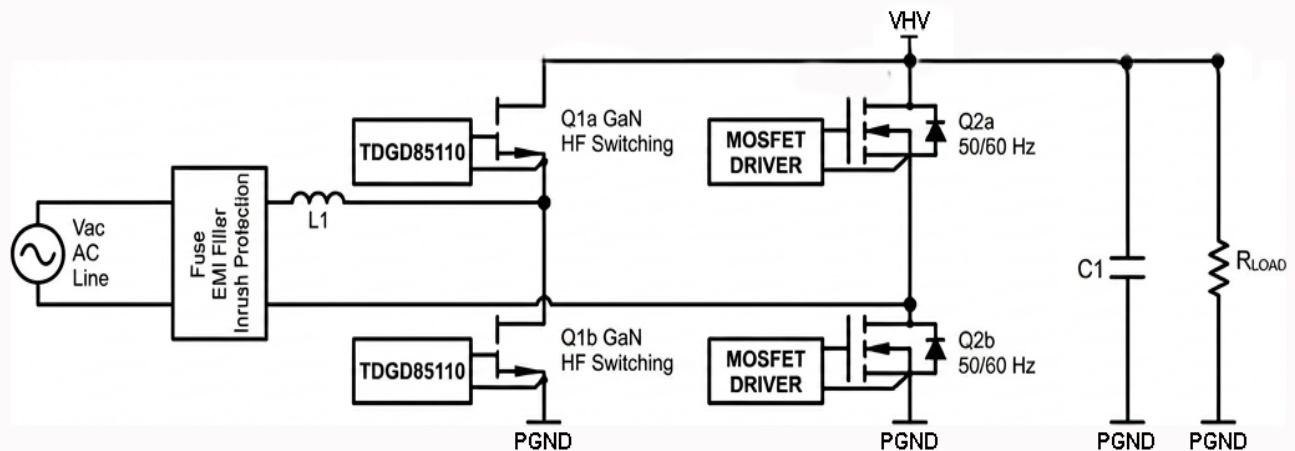


Figure 12: Totem pole PFC: TDGD85110EP as high and low side drivers

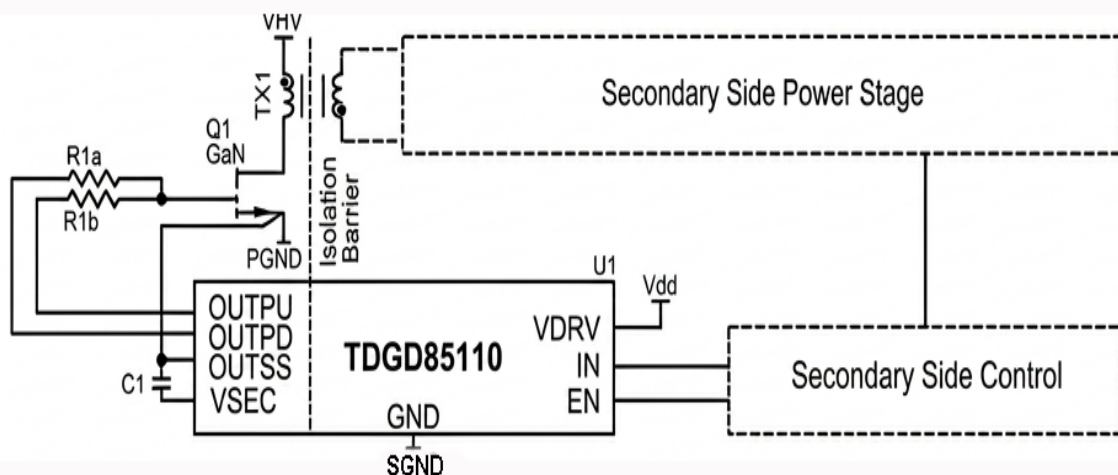


Figure 13: Secondary control to primary drive-TDGD85110EP single driver

Typical Applications

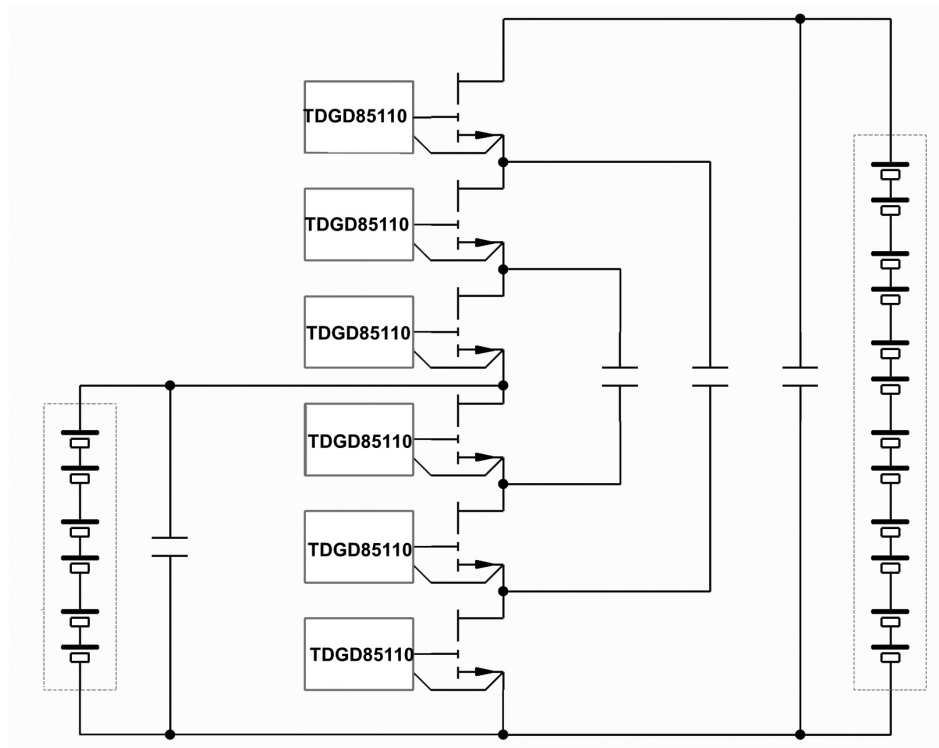


Figure 14: Multi-level converter: Stacked low-voltage switches results in higher efficiency. TDGD85110EP makes this easy to drive.

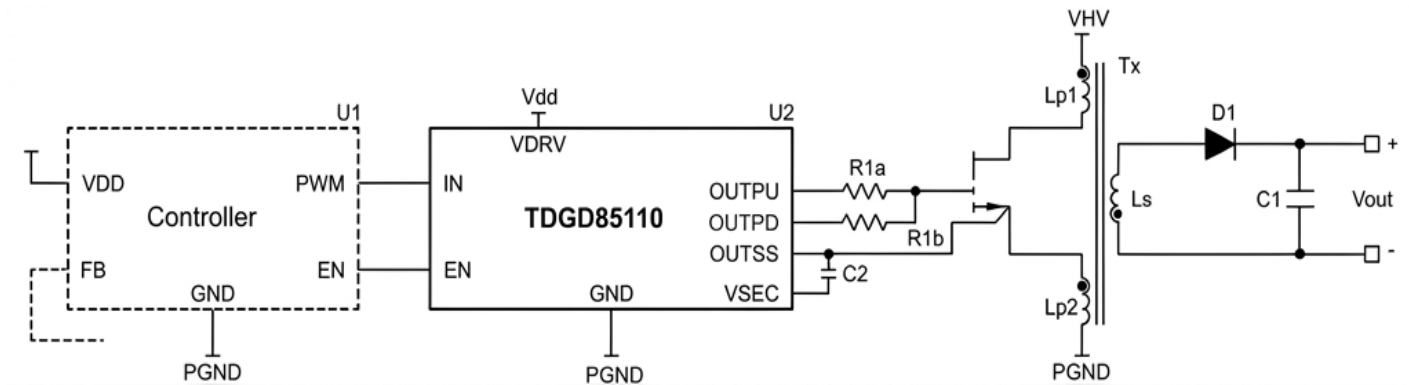


Figure 15: Center-switched flyback: TDGD85110EP driving center-tapped switch (symmetrical bipolar voltage swings for reduced Common-Mode noise)

Typical Application Example

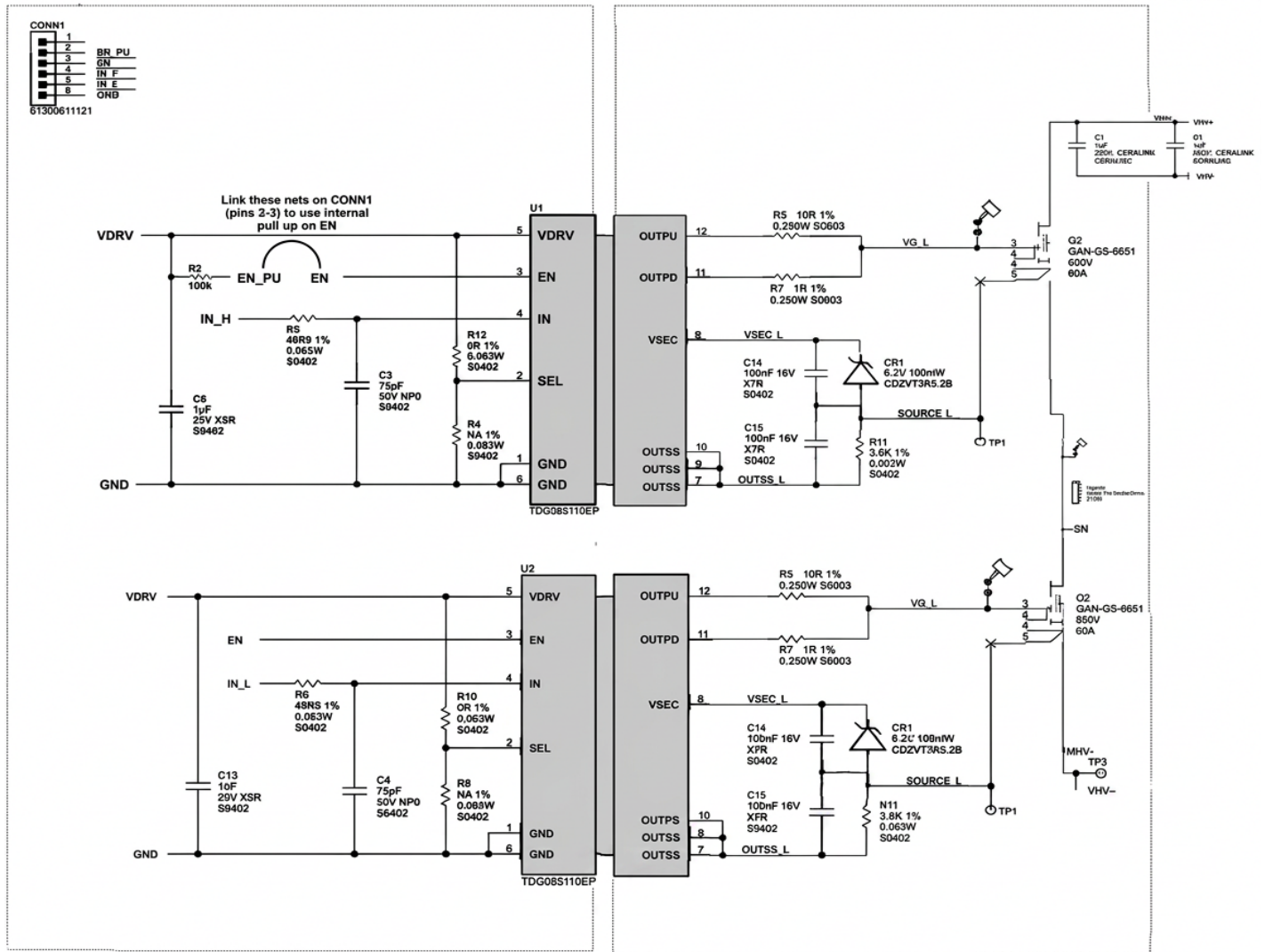


Figure 16: TDGDEK85110KNH-01-T-MH schematic for driving a GaN transistor with a bipolar drive arrangement. TDGDEK85110KNH-01-T-MH is a design example for half bridge gate driver with GaN transistors. There is also a bipolar output drive configuration for additional protection against false turn-on events. The design parameters are shown in Table 1.

Table 1: Design Parameters

Parameter	Value	Units
DRV	10.8 - 13.2	V
Maximum Switching Frequency	1000 _[1]	kHz
SEC	50	nF
SEC_RIPPLE	5-10	%

^[1] Frequency depends on factors like heat sinking, temperature, high voltage decoupling capacitance and IN PWM duty cycle range.

PCB Layout Considerations

Layout Guidelines

The following are some key points to consider while doing the PCB layout for the best performance with TDGD85110EP:

- Place the TDGD85110EP gate driver as close as possible to the transistor. This is necessary to minimize the path of the high peak currents. This arrangement will also minimize the loop inductance and noise injection on the gate signals.
- Ensure that the resistors connected between the isolated output drive pins to the gate of the transistor are high power rated and have high power surge withstanding capability.
- Decoupling capacitors must be connected close to the VDRV/GND and VSEC/OUTSS pin-pairs.
- The path connecting to the source of the transistor should be minimized to avoid large parasitic inductances

The layout should have good thermal relief to help dissipate heat from the gate driver to the PCB. It is recommended to use vias to maximize thermal conductivity. Further detailed PCB layout guidelines are available in the Teledyne HiRel application note AppN85110-9_072026, "Minimizing PCB Parasitic Effects with Optimum Layout of the Gate Driver Loop Applicable to TDGD85110EP Gate Drivers."

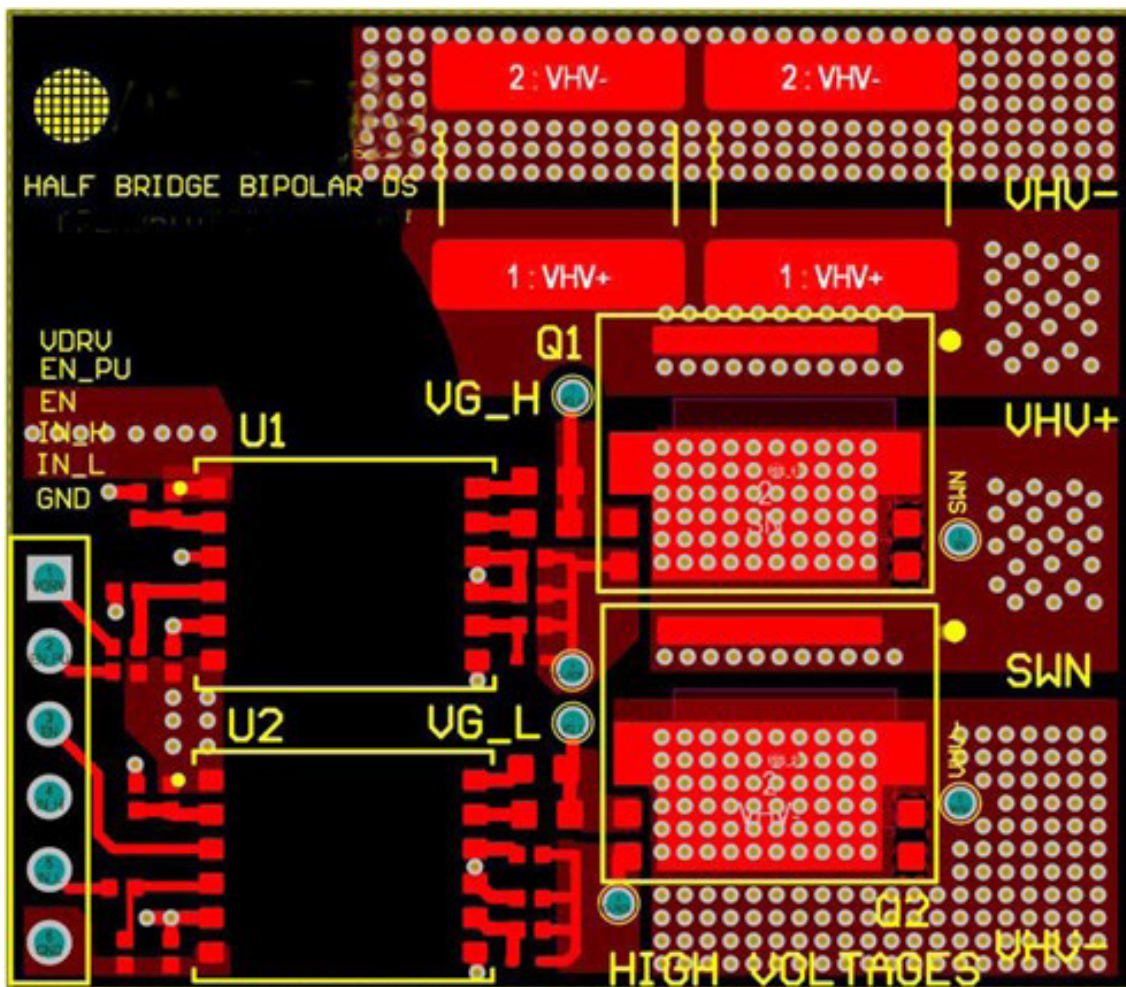


Figure 17: Example PCB layout

System Immunity to External Transients

During various system-level events, large transient currents can flow for short periods. Examples of this include lightning surge testing to IEC61000-4-5, and system-level ESD testing to IEC61000-4-2. During these events, the large transient currents that flow can also create large stray magnetic fields, and these can also couple unintentionally to the isolated gate driver.

It is recommended to protect the driver enable (EN) pin to achieve a power-train “safe-state” during such external transient events. An example of the use of this safe-state architecture is shown in Figure 18 for a Totem-Pole PFC power stage. When a surge event is detected, the system controller inhibits the PWM gate drive signal to both GaN and MOS legs, and also pulls down the open-drain Enable (EN) lines to all drivers. This puts the power-train into a safe state and ensures a robust response to the surge event.

For further details, refer to the application note Design and Application Guide for the TDGD85110EP.

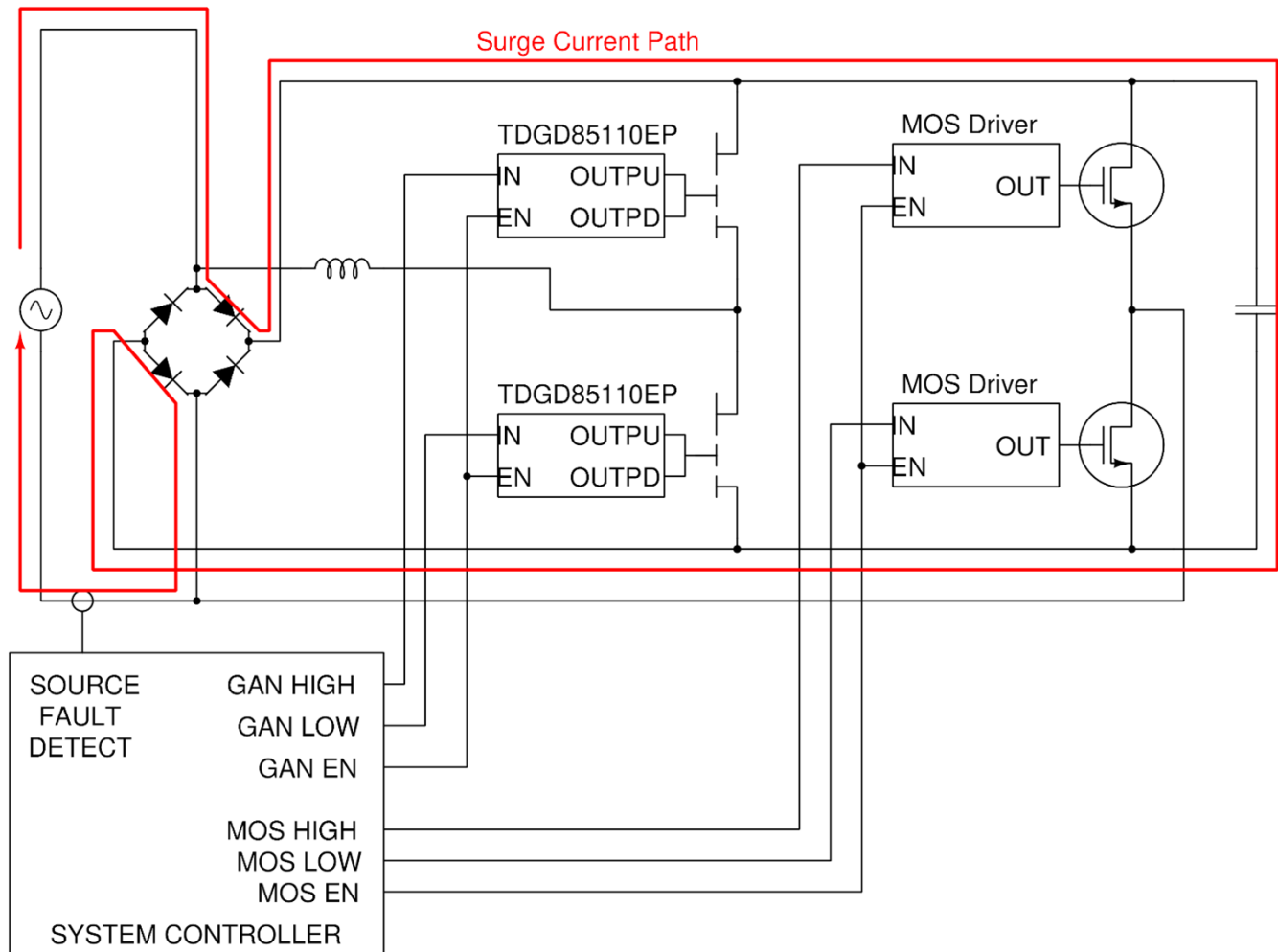
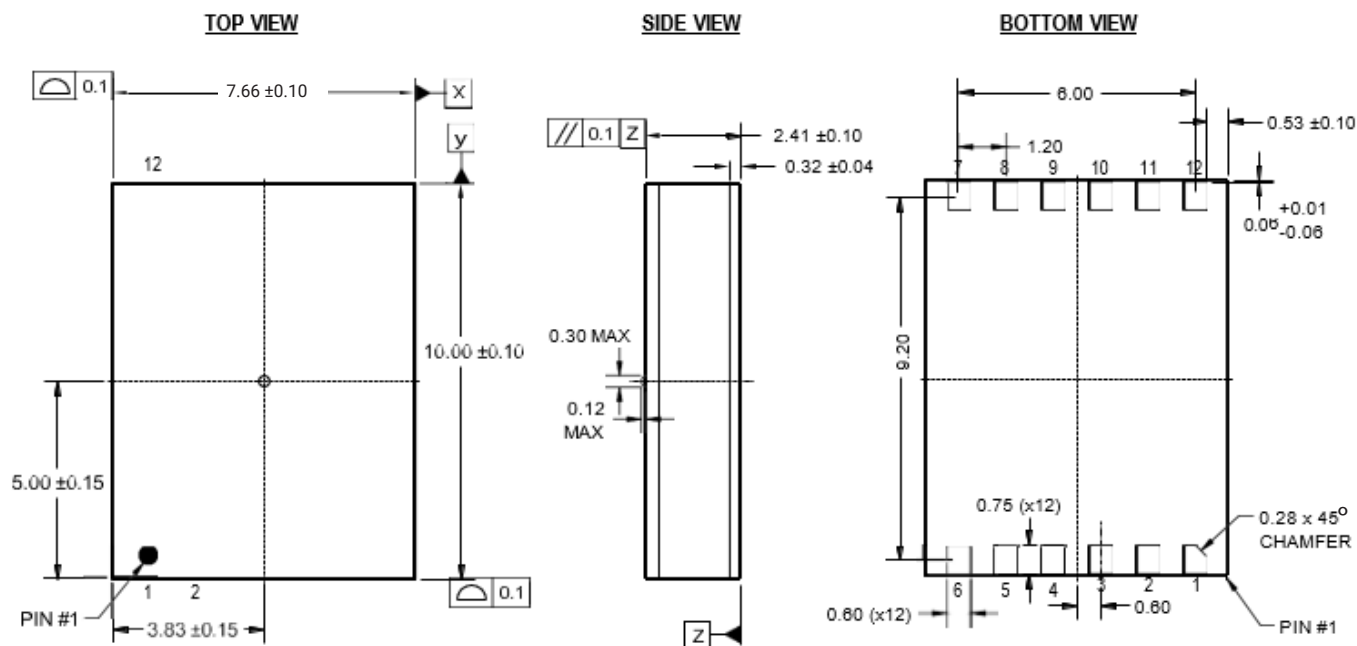


Figure 18: Block diagram of system level surge-detection inhibit signal used to disable isolated gate drivers using the EN pins

Package Outline Drawing

Outline Drawing - Low Profile SMT NOT TO SCALE

Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs,
and dambar protrusions Exact case and lead configuration
at supplier discretion within limits shown

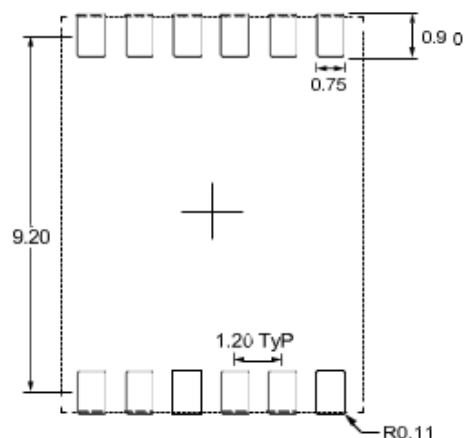


STANDARD BRANDING REFERENCE TOP VIEW



Line 1: Index + Part Number
Line 2: Logo, 4-digit Date Code
Line 3: Assembly Lot Number

PCB LAYOUT REFERENCE VIEW



Reference Land Pattern Layout.

All pads are a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances (reference EIA/JEDEC Standard JESD51-5)

Figure 19: TDGD85110EP NH Package Outline

Revision History

Document Number	Release Date	Description
TDGD85110EP_06_2026 Rev -	06_30_2026	Initial Release / Product Specification